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09/887,913	06/20/2001	Jeffrey Lukanc	IDT-1616	7471

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BEVER, HOFFMAN & HARMS, LLP
1432 CONCANNON BLVD
BUILDING G
LIVERMORE, CA 94550-6006

EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,913	LUKANC, JEFFREY	
	Examiner	Art Unit	
	Guy J. Lamarre	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .....

Response to Amendment

* This office action is in response to Applicants' **Amendment** of *16 March 2006*.

* Claims 1-22 remain pending.

* The prior art rejections of record are maintained in response to Applicants' amendment.

Response to Arguments

* Applicants' arguments have been fully considered but they are not persuasive because the prior art of record does restrict application of the dedicated bus as alleged. **Whetsel** (US Patent No. 6408413; filed 18 Feb. 1998) also discloses dedicated bus as claimed.

Claim Rejections - 35 USC ' 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

1.1 Claims 1-22 are rejected under 35 U.S.C. 102 (e) as being anticipated by **Whetsel** (US Patent No. 6408413; filed 18 Feb. 1998).

Whetsel discloses equivalent built-in-self-test for integrated circuits in e.g. Fig. 2 and related description and Abstract, comprising plural memory blocks (MM1-3), plural test modules coupled to said memory blocks (TAP1-3), dedicated line/bus (TDI line 26), and related coupling means to effect mode switching.

Whetsel discloses that '*[I]n FIG. 5 it is seen that TAPs 2-4 have multiple scan inputs. In particular, the TAPs 2-4 have scan inputs as follows: TAP2 has TDI pin 26 and TDO1; TAP3 has TDI pin 26, TDO1 and TDO2; and TAP4 has TDI pin 26, TDO1, TDO2 and TDO3. This is to allow for serially concatenating enabled TAPs together in different ways. For example TAP1*

and TAP4 can be enabled at the same time and linked together into the serial path between TDI 26 and TDO 27. In this arrangement, TAP1 and TAP4 can participate together during test while TAP2 and TAP3 are disabled. The Link Control signals LC2-4 to TAPs 2-4 select the appropriate scan input to the TAPs to make a particular serial link between TAPs. TLM 51 can provide the following TAP linking arrangements between TDI 26 and TDO 27....'

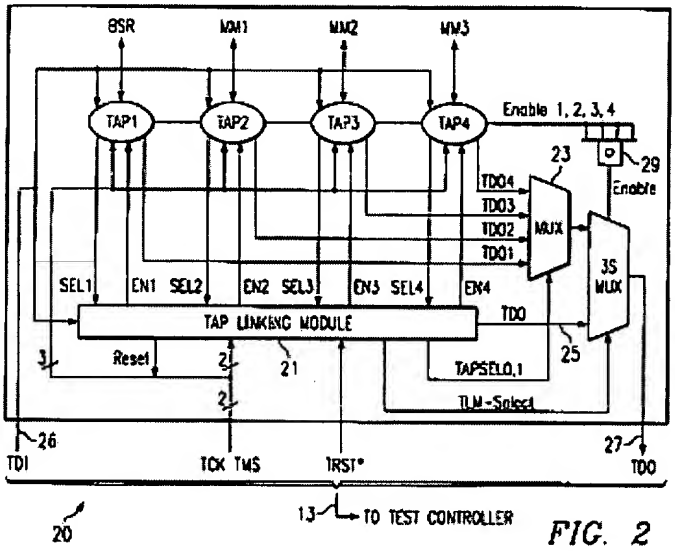

FIG. 2

Claim Rejections - 35 USC § 103

2. **Claims 1-3, 5-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over (US Patent No. 6587979) to **Kraus** and **Cowles** (US Patent No. 6212114; filed Jul. 1, 1999).

As per Claims 1-3, 5-22, Kraus substantially discloses the claimed built-in-self-test for integrated circuits in e.g. Fig. 12 and col. 5 line 7 et seq., comprising plural memory blocks (Figs. 5-12, 16), plural test modules coupled to said memory blocks(Figs. 5-12, 16), data/test line/bus (Figs. 5-12, 16), and related coupling means to effect mode switching, viz, *'A test system in accordance with the invention includes a built-in self-test (BIST) circuit incorporated into an integrated circuit (IC) for testing one or more random access memories (RAMs) of varying size embedded in the IC. During normal circuit operation logic circuits implemented within the IC read and write access the RAMs. During a RAM test, the*

BIST system disconnects the logic circuits from the RAMs and connects internal test circuits to the RAMs I/O ports to enable them to test the RAMs.'

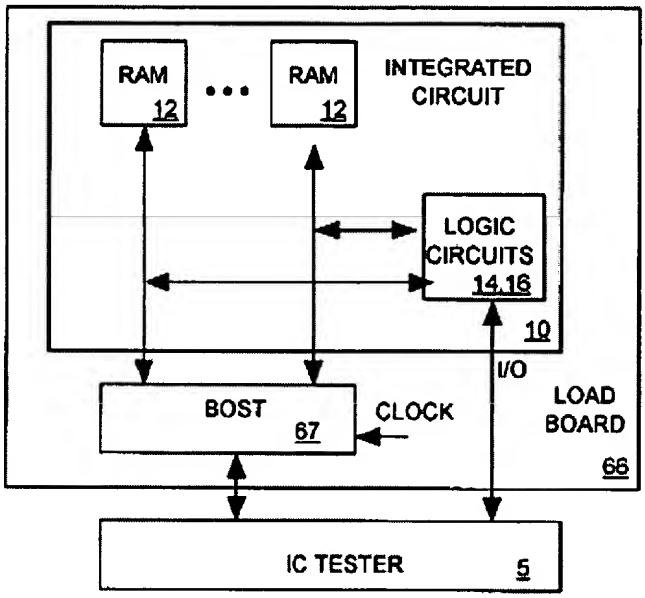

FIG. 12

Not explicitly disclosed in detail in **Kraus** is a dedicated test bus.

However, Cowles (US Patent No. 6212114; filed Jul. 1, 1999) in an analogous art discloses such dedicated test bus structure approach, e.g., in col. 2 lines 1, 62; col. 6 line 31, col. 9 line 32.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the testing procedure in **Kraus** by including therein a dedicated test bus structure approach as taught by **Cowles,** because such modification would provide the procedure disclosed in **Kraus** with a technique whereby a single dedicated test bus, as opposed to plural test buses, is employed in testing plural memory blocks so as to optimize circuit overhead. {See **Cowles**, col. 9 lines 32-35 et seq.}

3. **Claim 4 is** rejected under 35 U.S.C. 103(a) as being unpatentable over (US Patent No. 6587979) to **Kraus, Cowles** (US Patent No. 6212114; filed Jul. 1, 1999) and **Nadeau-Dostie et**

al. (US Patent No. 5812469).

As per Claim 4 , Kraus and **Cowles** substantially disclose the claimed built-in-self-test for integrated circuits for memory system, but fail to explicitly disclose in detail that testing can also be applied to multiport or dual port memories. **However, Nadeau-Dostie et al.,** in an analogous art, discloses a *dedicated test procedures,"* wherein such techniques are described {See **Nadeau-Dostie et al.,** Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Kraus** and **Cowles** by including therein multiport or dual port memory testing technique as taught by **Nadeau-Dostie et al.,** because such modification would provide the procedure disclosed in **Kraus** and **Cowles** with a technique providing testing is flexible, e.g., *'An advantage of the present invention is allowing testing for the shorts of interest in such a way that the same algorithm used for single-port memories can be used and that the test address and data can be easily generated from a single bus, irrespective of the number of ports, reducing considerably test time and implementation cost.'* {See **Nadeau-Dostie et al.,** Abstract.}

As per Claim 16, Cowles discloses data/test signal broadcasting in col. 9 line 49, col. 7 line 54 & 62, col. 8 line 38.

As per Claims 20-22, Cowles discloses means to identify and apply test/data/clock signals to the memory blocks, e.g., at col. 9 line 49, col. 7 line 54 & 62, col. 8 line 38.

4. Claims 1-3, 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,568,437 to Jamal and **Kraus et al.** (US Patent No. 6587979) and **Cowles** (US Patent No. 6212114; filed Jul. 1, 1999).

Referring to claim 1, Jamal discloses the built-in-self-test for integrated circuits having read/write memory. Jamal teaches to use "an integrated circuit 80" with random access memory (RAM)" 84 (see e.g. abstract, line 1 and Fig. 2a), "the built-in self tester (test module) 100" for the RAM (see e.g. abstract, line 2 and Fig. 2a), and "a bus" (see "the RAM BIST controller 102

/see Fig. 4/ generates test data for the RAM 84 and transmits it over the data bus ... /see column 5, lines 11, 12/).

Jamal does not explicitly point out to multiplication (integration) of the elements, but Jamal does not limit such well known feature, inherently teaching for using of any degree of element integration inside the chip, that is well known in the integrated circuits (IC) industry.

However Kraus et al., in an analogous art, discloses a memory *wherein* such techniques are described. {See **Kraus et al. ,** Id., Fig. 12 and dedicated bus in col. 2 line 54 et seq.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in Jamal by including therein a RAM multiplicity technique as taught by **Kraus et al. ,** because such modification would provide the procedure disclosed in **Jamal** with a technique whereby data bus is made reusable so as to optimize circuit overhead. {See **Kraus et al.,** col. 2 line 54 et seq.}

Not explicitly disclosed in detail in **Kraus/ Jamal** is a unique dedicated test bus.

However, Cowles, in an analogous art discloses such dedicated test bus structure approach, e.g., in col. 2 lines 1, 62; col. 6 line 31, col. 9 line 32.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the testing procedure in **Kraus/ Jamal** by including therein a dedicated test bus structure approach as taught by **Cowles,** because such modification would provide the procedure disclosed in **Kraus/ Jamal** with a technique whereby a single dedicated test bus, as opposed to plural test buses, is employed in testing plural memory blocks so as to optimize circuit overhead. {See **Cowles**, col. 9 lines 32-35 et seq.}

Claims 2-3, 5-10 depend from respective claim 1, hence inherit the rejection in claim 1. Also, according claims 2, 3, Jamal teaches to use pads (see, for example, "in this technique, multiplexers provide paths from IC input/output (I/O) pads to the targeted subcircuit" /column 1,

lines 18-20/), and "an integrated circuit, wherein the RAM BIST controller comprises switching logic which, in response to signals, decouples said BIST and said RAM from other components on the integrated circuit and couples said BIST RAM controller to the RAM" (column 10, lines 45-50).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use and/or modify Jamal switching means, because one of ordinary skill in the art would use well known Jamal's switching principles in order to provide the coupling, for example, the test bus and the circuitry.

Referring to claim 5, Jamal teaches that "the RAM BIST controller 102 generates test data for the RAM 84 and transmits it over the data bus of width WD. The controller 102 also transmits control signals to the RAM over control line of width Wc to addresses within the RAM. The addresses are specified by the RAM BIST controller 102 and transmitted to the RAM 84 over the address line of WA" (column 5, lines 11-15), and "a latch enable signal commands a BIST register to latch the address of the malfunctioning location in the RAM 84" (column 4, lines 29, 30).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal's standard lines or modify them, because one of ordinary skill in the art would use well known address/data/control signal interchange technique in order to provide signal communication between means.

According to claim 6, Jamal discloses that the "generated test enable signals switch the multiplexers into test mode (column 1, lines 20, 21). Upon receipt of the scan mode enable signal, the BIST can receive initialization data through a "scan in" line, or the BIST (column 4, lines 4-6).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal's line or modify it, because one of ordinary skill in the art would use transmitting line for transmission of well known enable signals to the test modules, considering well known and obvious use of the enable signal transmitting technique.

Referring to claim 7, Jamal discloses that the "the RAM BIST controller controls the RAM during a test where the RAM includes data, address, and control lines" (column 2, lines 54-56).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal's line or modify it, because one of ordinary skill in the art would use transmitting line for transmission of well known data value, considering well known and obvious use of the data transmitting technique.

According claim 8, Jamal discloses "unique address", data storage" (column 2, line 31), and that the "data storage locations, and each location has a unique address" (column 2, lines 30, 31), and "the input/output circuitry includes a register capable of storing address, data, and control signal information of a read/write memory ..." (column 2, lines 40-43). Also Jamal teaches that "the BIST IIO is ... capable of storing an address of a data storage location in the RAM ..." (column 2, lines 60-62), and "A test mode or test enable signal is received by a RAM BIST controller 102 initializes registers within the RAM BIST controller 102 ..." (,column 5, lines 3-5).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal's data storages and "unique address", because one of ordinary skill in the art would simply use or modify well known and obvious address storing technique in order to provide storing of "unique address".

Referring to claim 9, Jamal discloses that the "multiplexer or "functional block" isolation is one approach to testing these subcircuits. In this technique, multiplexers provide paths from IC input/output (IIO) pads to the targeted subcircuit"(column 1, lines 17-20), and "functional block isolation suffer from several disadvantages, however, including multiplexer delays, routing congestion, and the need for externally generated test vectors or signals" (column 1, lines 21-24).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal's multiplexing principles and multiplexers or modify them, because one of ordinary skill in the art would use well known multiplexers for routing signals from the corresponding blocks, considering well known and obvious multiplexing technique.

Claims 2-9 are rejected as depended from respective claim 1, hence inherit the deficiency in claim 1.

5. Claims 10-18 are rejected under 35 U.S.C. 103(x) as being unpatentable over US 5,568,437 to Jamal/**Kraus et al./ Cowles** in further view of US 5,515,540 to **Grider et al.**

Referring to claim 10, Jamal/**Kraus et al./ Cowles** discloses RAM and does not explicitly point out and limit RAM capacity, inherently teaching for using of any reasonably applicable kinds of RAMs and their capacities. Besides, RAM memories are in general known to be expandable and the prior art does not have to show intended use. Grider et al. teaches that "the embedded address and data busses are used on the DS5000FP to connect to external byte-wide memory devices. Pins AO-A14 address up to 32 Kbytes of Program/Data memory which is transferred over pins EDO-ED7 (a bidirectional port). An additional 32 Kbytes of data memory (cannot be used for program memory) can be addressed by using ECE2* (manipulation of ECE2* is described in the DS5000 data sheet)" (column 6, lines 50-57).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Jamal/**Kraus et al./ Cowles** with the teaching of Girder et al. by simply using RAM with the limited capacity, because one of ordinary skill in the art would easier use the smaller RAM's capacity in order to achieve higher reliability.

According claim 11, Jamal discloses that "during normal mode, the RAM 84 may be connected to other system signals through the BIST 100. In other words, BIST circuitry 100 interfaces the RAM 84 to other components on the integrated circuit ..." (column 6, lines 59-62), and "the RAM BIST controller controls the RAM during a test [test mode] where the RAM includes data, address, and control lines Jamal, disclosing RAM, does not explicitly point out and limit RAM capacity, inherently teaching for using of any reasonably applicable kinds of RAMs and their capacities, but Grider et al. teaches that "the embedded address and data busses are used on the DS5000FP to connect to external byte-wide memory devices. Pins AO-A14 address up to 32 KBytes of Program/Data memory which is transferred over pins EDO-ED7 (a bidirectional port). An additional 32 Kbytes of data memory (cannot be used for program memory) can be addressed by using ECE2* (manipulation of ECE2* is described in the DS5000 data sheet)" (column 6, lines 50-57).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Jamal with the teaching of Girder et al. by simply using normal and test modes for 32 Kbytes RAM operation, because one of ordinary skill in the art would easier use well known and obvious access to the RAM in normal functional regime and in the test regime in order to provide the normal operation and testing of the random access memory.

Referring to claim 12, Jamal discloses that "the controller 102 also transmits control signals to the RAM over control line of width Wc ..." (column 5, lines 12-14). Also, Grider et al.

teaches that "memory ... include the ability to address 128K bytes of NV SRAM on the bytewide bus, multiple memory architectures for optimum

implementation, and a peripheral memory map" (column 8, lines 47-50).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal with the teaching of

Girder et al. by simply using test control line (bus), because one of ordinary skill in the art would use the test control line (bus) during the test regime (mode) in order to provide testing operation of the memory.

Referring to claims 13, 14, the examiner interprets claims 13 and 14 as being similar to claims 8 and 2 respectively, therefore claims 13 and 14 are rejected based on the same rationale thereof.

Referring claim 15, Jamal teaches that the "BIST controller" controls the pad switching (column 10, line 45). Jamal does not call his "BIST controller" as JTAG, but provides "BIST controller" with the analogous functions.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal's BIST controller, because one of ordinary skill in the art would use the any type controller, providing analogous controlling functions for coupling of the pads in order to switch system circuitry during normal or test modes.

According claims 16, 17, Jamal describes "an integrated circuit with read/write memory and an improved read/write memory self testing capability" (column 2, lines 26-28), and teaches that "the method includes activating a read/write memory location on the integrated circuit and activating a built-in self tester (BIST) on the integrated circuit. The BIST writes test data to the memory location and reads the test data as retrieved data from the same memory location'

(,column 2, lines 66, 67 and column 3, lines 1-3). Also, Grider teaches to use "Embedded Bus ReadWrite" (column 6, line 44).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal/**Kraus et al./ Cowles** with the teaching of Girder et al. by simply using test bus, because one of ordinary skill in the art would use the test control line (bus) during the test regime (mode) in order to provide writing/reading operation of the RAM blocks.

Cowles discloses data/test signal broadcasting in col. 9 line 49, col. 7 line 54 & 62, col. 8 line 38.

According to claims 18-19, Jamal teaches that "the test clock signal clocks the BIST circuitry 12 and testing operations performed by the BIST on the RAM 14 (column 1, lines46-48), and "a "scan clock" line produces a clocking signal for the scan in or shift in operation" (column 4, lines 7, 8).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal's "clocking signal", because one of ordinary skill in the art would use well known timing principles, considering well known and obvious methods for bus operating in response to clock signal during the selected mode.

As per Claims 20-22, Cowles discloses means to identify and apply test/data/clock signals to the memory blocks, e.g., at col. 9 line 49, col. 7 line 54 & 62, col. 8 line 38.

Conclusion

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
6/12/2006